

WHAT IS CLAIMED IS:

5

1. A voltage generating circuit that generates an output voltage according to an input voltage, the voltage generating circuit comprising:

10 a resistor circuit that is serially implemented with respect to the input voltage;

a condenser unit that cooperates with the resistor circuit to generate the output voltage;

15 a digital delay circuit that delays at least one of a rise and a fall of the input voltage and generates a delay output based thereon; and

a bypass circuit that controls bypassing of a predetermined resistor included in the resistor circuit according to the delay output of the digital delay circuit.

20

2. The voltage generating circuit as claimed in claim 1, wherein:

25 the resistor circuit includes a plurality of resistors that are serially connected; and

the bypass circuit establishes parallel connection with the predetermined resistor that is to be bypassed, and includes a switch that is switched according to the delay output of the digital delay circuit.

30

3. The voltage generating circuit as claimed in claim 1, wherein:

the delay output of the digital delay circuit  
5 controls the bypassing of the predetermined resistor to be performed for a period of time during which the output voltage generated according to the input voltage is rising to a predetermined voltage.

10

4. The voltage generating circuit as claimed in claim 1, wherein:

15 the bypass circuit controls bypassing of a plurality of resistors included in the resistor circuit according to delay outputs of a plurality of digital delay circuits having differing delay times.

20

5. A method of generating an output voltage according to an input voltage, wherein a resistor circuit  
25 is serially implemented with respect to the input voltage, the method comprising the steps of:

delaying at least one of a rise and a fall of the input voltage and generating a delay output based thereon;

30 controlling bypassing of one or more resistors included in the resistor circuit according to the delay output; and

adjusting a rise of the output voltage during

bypass of the one or more resistors.